BANYAN SWITCHED PROCESSOR DATAPATH

ABSTRACT

A data-processing system comprises a register file, a routing unit, a Banyan switch, a switch control unit, a constant generator, and an arithmetic logic unit. The arithmetic logic unit comprises a bitwise function unit, pipeline register, and an accumulator. The Banyan switch may have an internal bitwidth of w and comprise N switching stages. N may equal $log_2(w)$ or $log_4(w)$. In the case of $log_2(w)$ stages, each switching stage has N/2 switching cells. The routing unit comprises a control logic that generates a control signal, and various logics that respectively operate on various bit groups of the control signal. The switch control unit comprises a shift constants generator, a pipeline flip-flop, and a switch tree. A data-processing method implemented by the above system is also disclosed.